

REMARKS

The Applicant's representative has carefully reviewed and considered the Office Action mailed on July 30, 2001, and the references cited therewith. In this timely filed response, no claims have been canceled, amended, or added; as a result, claims 22-32, 59-61, and 63-70 are now pending in this application.

§102 Rejection of the Claims

Claims 22-32, 59-61, and 63-65 were rejected in § 4 of the Office Action under 35 U.S.C. § 102(e) as being anticipated by Manning (U.S. Patent No. 5,610,864). The MPEP requires that "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." See M.P.E.P. § 2131. Therefore, the Applicant respectfully traverses this rejection by the Office.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in another Office Action mailed to the Applicant on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to substantially similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support using a mode control signal for *switching* or *selecting* between burst and *pipelined* modes of operation, as claimed in claims 22, 23, 59, 60, 61, 63, 65, and 66? What text in Manning, for example, supports the Office Action statement that "Manning discloses a memory circuit, comprises [sic] control logic for providing a *mode control signal indicating a pipelined mode* or a burst mode of operation", made with respect to claim 65?

Second, the Office Action has failed to produce a *prima facie* case of anticipation. The only references offered to support the assertion that Manning "discloses the invention as claimed" with respect to claim 22 are: Fig. 1, Refs. 18, 38, and 40; Fig. 5, Ref. 66; col. 4, line 19; col. 5, lines 43-50; col. 6, lines 14-32; col. 7, lines 43-54; and col. 8, lines 58+). Fig. 1, Ref. 18 is a latch for signals and addresses, not a multiplexer, as stated in the Office Action. Ref. 38 is generic DRAM control logic. Ref. 40 is a block "mode register", with no indication regarding exactly which modes may be operative, or how they are selected. Fig. 5, Ref. 66 is a write timing circuit, used to latch R/W signals, and not to multiplex addresses, as stated in the Office Action. Col. 4, line 19 merely confirms the function of the latch 18. Col. 5, lines 41-50 discuss

the possibility of using a pipelined architecture as an *alternative* to burst operation, but not as enabling the *selection or switching* of pipeline or burst operations within the *same* memory. Col. 6, lines 14-32 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Finally, col. 8, lines 58+ merely discuss burst R/W operations. Manning gives no support whatever in any of these references to the idea that a pipelined mode of operation is the same as a fast page mode. Thus, it is impossible for Manning to disclose the ability to *select or switch* between burst and *pipelined* modes of operation, as claimed by the Applicant in independent claim 22, as well as in independent claims 59, 60, 61, 63, 64, 65, and 66, and all of the claims which depend from them.

Third, other statements in the Office Action respecting the teachings of Manning do not comport with the specific wording of the claims in the instant application. For example, with respect to claims 23-25, statements are made that Manning discloses "external mode select signal", "write enable", and "a counter". In reality, the mode select signal in Manning (which does not operate to switch to a pipelined mode, as claimed by the Applicant), is *internal* to the circuitry of Fig. 1. Similarly, the write enable signal of Manning is never used for "switching the memory circuit between a burst mode and a pipelined mode" as claimed by the Applicant; rather, it is merely used start/stop burst access cycles. Finally, the statement "Manning discloses a second external address" fails to disclose that the address is not "for operating in the pipelined mode" as claimed by the Applicant, rather it is for operating in the burst mode (see col. 4, lines 22-49). A further example includes the statement "Manning ... discloses no CAS delay latency ...", whereas the Applicant claims no CAS latency during a *pipelined* write cycle in claim 30. Still another example includes the statement for claim 64 that "Manning discloses a counter", which fails to note that the counter is not "connected between the control logic and the first and second multiplexers" as claimed by the Applicant. This statement also points to a contradiction - the Office Action refers to the counter of Manning (26) as both a counter, and a multiplexer, which is impossible, at least if it is connected as claimed by the Applicant.

In short, what is taught by Manning is not identical to the subject matter of the present invention as required by the M.P.E.P., and therefore, the rejection is improper. Reconsideration and allowance of claims 22-32, 59-61, and 63-65 is respectfully requested.

§103 Rejection of the Claims

Claims 22-32, 59-61, 63-65, and 66-72 were rejected in § 6 of the Office Action under 35 U.S.C. § 103(a) as being unpatentable over the article "Burst DRAM Function and Pinout", Oki Electronics Ind. Co., Ltd (Oki), JC42.3, Albuquerque, 2nd Presentation, item #619, September 1994 in view of Manning (U.S. Patent No. 5,610,864). The Applicant respectfully traverses this rejection by the Office.

To establish a prima facie case of obviousness, the references themselves must provide a suggestion or motivation for combination. MPEP §2143.01. References must be considered in their entirety, including parts that teach away from the claims. MPEP 2141.02. "Obvious to try" is not a proper standard for determining obviousness. *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir., 1988). "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed Cir., 1988).

First, while the Office Action asserts that it is obvious to incorporate a "multiplexer for switching the memory circuit between a burst and a pipelined mode" from Manning into the device disclosed by Oki, it should be noted from the discussion above that the Applicant's representative was unable to find anything in Manning which discloses such a "multiplexer". Thus, it is respectfully requested that Manning's teaching of such a device be designated with more specificity. And while the purported reason to combine the references in this case is to "provide high speed data access and compatibility with industry standards and protocols", no such language or suggestion is found in the Oki reference. The Applicant's representative could also find no reason why adding the functions or structure of the Oki device would serve to improve Manning's invention. Thus, no motivation to combine the references is provided.

Further, even if the "selection and temporary storage circuit" along with the "multiplexer" of Manning were to be incorporated into the device disclosed by Oki, there is no reason to believe that such a device would function to switch "the memory circuit between a burst and a pipelined mode of operation" as asserted in the Office Action. As noted above, there is no such multiplexer, and Manning (along with Oki) completely fails to teach *switching or selecting* a pipelined mode of operation in a memory that also provides burst operation. Since there is no such "multiplexer", such a combination would be inoperative.

Additionally, the Applicant is unable to find, and the Office has failed to show, how combining Oki with Manning serves to teach each and every element of the instant invention. See M.P.E.P. § 2142. As discussed previously, Manning fails completely to disclose *switching* between burst and *pipelined* modes of operation. The Office admits that Oki also fails to disclose *switching between burst and pipelined modes*, or even circuitry to select and store a first external address. The Applicant also contends that Oki fails to teach the third element of claim 66: control logic for providing a selected mode control signal (where the mode control signal is received and used to switch the memory circuit from a pipelined mode to a burst mode). Since Oki does not teach any of the elements of claim 66, no combination of Oki and Manning can supply the missing elements of the Applicant's invention which enable *switching* between burst and *pipelined* operation. This argument applies with equal force to independent claims 22, 59-63, and 65-66, along with all of the claims which depend from them.

Second, as noted above, other statements in the Office Action respecting the teachings of Manning do not comport with the specific wording of the claims in the instant application. For example, with respect to claims 23-24, it is asserted that "Manning further discloses external mode select signal", which is contradicted by the admission that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in another Office Action mailed to the Applicant on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. With respect to claim 28, it is asserted that "Manning further discloses a second external address", but not that the address is for operation in a pipelined mode, as claimed by the Applicant. A further example includes the statement "Manning ... discloses at least two CAS latency during a read cycle ...", whereas the Applicant claims at least two CAS latency during a *pipelined* read cycle in claim 31. With respect to the statements made in the Office Action for claims 67-70, the Office is referred to the remarks made in the previous section with respect to claims 23-25. The statement in the Office Action that "Manning discloses EDO mode" fails to note that Manning does not disclose switching between a burst EDO mode and a *pipelined* EDO mode, as claimed by the Applicant in claim 72.

Third, as mentioned in two previous responses to Office Actions in this matter, the Applicant cannot find where the term "fast page pipeline" proffered in the Office Action § 7 is

defined. As noted above, Manning gives no support whatever to the idea that fast page mode and pipelined mode are the same. Thus, the Applicant still fails to understand the meaning of this particular phrase, and looks to the Office for a more detailed explanation. Otherwise, the assertion that "Manning discloses mode circuitry to select between fast page pipeline and burst" is simply not supported by any of the teachings of Manning.

Fourth, the Applicant's representative has reviewed the Rossini reference mentioned in the Office Action at § 7. It should be noted that Rossini issued on June 7, 1995, which is less than one year before the application from which the instant application was divided, was filed (U.S. Patent Ser. No. 08/650,719, still pending, was filed on May 20, 1996). The Applicant reserves the right to file a Petition under 37 C.F.R. § 1.131 to swear behind the Rossini reference, if necessary. It should also be noted that Rossini merely reveals the ability of a cache controller to operate with various types of SRAM ("standard", "burst", or "pipelined burst"). Selecting between "burst and burst pipeline [modes of operation]" within the same memory is simply not disclosed, as asserted in the Office Action.

In short, what is discussed by Manning, Oki, and/or Rossini is not combinable to provide each and every element of the present invention, and therefore, the rejection is improper. Reconsideration and allowance of claims 22-32, 59-61, 63-65, and 66-72 is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Applicant's attorney at (612) 373-6913 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 30 day of October, 2001.

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